## ABSTRACT OF THE DISCLOSURE

A circuit to screen for defects in an addressable line in a non-volatile memory array comprises a current mirror circuit which has a plurality of mirroring stages. The current mirror circuit is connected to the addressable line and receives a control signal and mirrors the control signal to provide a current to the addressable line. In a preferred embodiment, the current mirror circuit provides a high voltage current to the addressable line which is used to effectuate an operation such as program or erase to the memory cells connected to the addressable line. The change in state or the absence of change in state of the memory cells connected to the addressable line can be used to screen for defects in the addressable line.